# Annual Technical Report

## SiC Discrete Power Devices

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13. ABSTRACT *(Maximum 200 words)*

A novel planar accumulation channel SiC MOSFET structure is reported. The problems of gate oxide rupture and poor channel conductance previously reported in SiC UMOSFETs are solved by using a buried P+ layer to shield the channel region. The fabricated 6H-SiC unterminated devices had a blocking voltage of 350 V with a specific on-resistance of 18 m$\Omega$-cm$^2$ at room temperature for a gate bias of only 5 V. This measured specific on-resistance is within 2.5X of the value calculated for the epitaxial drift region ($10^{16}$ cm$^{-3}$, 10 $\mu$m), which is capable of supporting 1500 V.

In addition, a novel planar lateral channel SiC high power JFET is described. Two-dimensional numerical simulations predicted low on-resistances with excellent current saturation and square FBSOA, which have been experimentally confirmed. A novel planar lateral channel SiC MESFET structure with vertical current flow in the drift region is also proposed and demonstrated by modeling and fabrication.

A hot wall chemical vapor deposition system has been constructed for the growth and doping of 6H- and 4H-SiC thin films at very high temperatures and high growth rates. The design incorporates a separate load lock to which a growth chamber and a RHEED chamber are attached.

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# Analysis and Optimization of the Planar 6H-SiC ACCUFET

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*Abstract:* This paper discusses the optimization of the planar 6H-SiC ACCUFET structure based upon analysis, simulations and experimental results. Two-dimensional numerical simulations demonstrate that the maximum electric field in the gate oxide can be kept below 3.5MV/cm even at the maximum blocking voltage of 1500V, by proper device design thereby eliminating the oxide rupture problem seen in SiC UMOSFETs. The trade-off between specific on-resistance and the maximum gate oxide electric field is obtained using simulations. The fabricated 6H-SiC unterminated devices had a blocking voltage of about 350V with a specific on-resistance of 18 m$\Omega$-cm$^2$ at room temperature for a gate bias of only 5V. This measured specific on-resistance is within 20% of the analytically calculated and simulated specific on-resistance for the same device. High temperature measurements show that the threshold voltage decreases with temperature and the accumulation channel mobility (~125 cm$^2$/V.s) is almost independent of temperature. The specific on-resistance exhibited positive temperature coefficient, as opposed to the undesirable negative temperature coefficient observed on previously reported high voltage SiC MOSFETs.

## I. Introduction

Silicon carbide power MOSFETs have a strong advantage over those made in silicon because the drift region can be thinner and have higher doping (for the same voltage rating) due to the higher breakdown electric field of SiC [1]. This translates into a 100 times lower specific on-resistance for SiC MOSFETs as compared to their Si counterparts. It has been shown that the MOS interface formed along the trench side walls is inferior to that formed on the Si-face of 6H-SiC [2] resulting in lower inversion layer mobilities along the trench side walls. This results in a high specific on-resistance for SiC UMOSFETs [3]. Another problem with the SiC UMOSFET is the gate oxide rupture caused by the higher electric fields in the SiC drift region. This problem is aggravated at the trench corners leading to catastrophic failure of the gate oxide at higher drain voltages [4], thus restricting the maximum operating voltage to less than half of the ideal breakdown voltage. All these obstacles have resulted in the fabricated SiC MOSFETs having specific on-resistances much higher than the ideal drift region values. Recently, high voltage 4H-SiC UMOSFETs were reported [5] which can block up to 1100V. However, due to low inversion channel mobility (1.5 $cm^2/V.s$), these devices had very high specific on-resistance of 433 $m\Omega$-$cm^2$ at 300K which is 125 times higher than the ideal calculated epitaxial layer specific on-resistance. DIMOS transistors on 6H-SiC with a BV of 760V and a specific on-resistance of 125 $m\Omega$-$cm^2$, which is 11X higher than the ideal value of the drift region, have also been reported [6]. The problems of high electric field in the gate oxide and the low channel (inversion layer) mobility have not been fully addressed with this structure. It is well known that, the accumulation layer mobility is much higher than the inversion layer mobility in silicon. Hence, assuming that the same applies to SiC, the low inversion channel mobility problem can be avoided if we use an accumulation channel, preferably on the Si-face. In a previous paper, we have proposed and experimentally demonstrated a planar vertical SiC ACCUFET structure which eliminates both the problems of premature oxide breakdown and low inversion channel mobility [7]. In this paper, the design and optimization of the 6H-SiC ACCUFET is discussed based upon analytical models, simulations and experimental results.

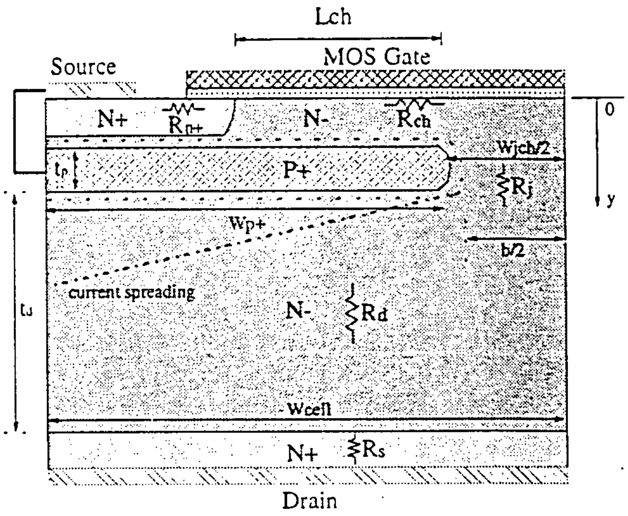

Fig.1 Schematic cross-section of the planar accumulation channel SiC vertical MOSFET. The buried $P^+$ is shorted to the source in the third dimension.

## II. Device Structure and Operation

The basic structure of the planar ACCUFET is shown in Fig.1. In this structure, a thin N-type region is formed below the MOS gate by using a buried $P^+$ implanted layer resulting in an accumulation channel FET. If the threshold voltage of the ACCUFET, ($V_{ta}$ ) is defined as the gate voltage at which the bands are flat at the $SiO_2$/SiC interface, it can be expressed as:

$$V_{ta} = V_{bi} - V_p - V_n + \phi_{ms} - Q_{ox}/C_{ox} \qquad (1)$$

where $V_{bi}$ is the built in voltage of the $P^+$-$N^-$ junction, $V_p$ and $V_n$ are the voltage drops in the $P^+$ and $N^-$ regions due to the band bending caused by the built in potential, $\phi_{ms}$ is the difference in the metal and semiconductor work functions, $C_{ox}$ is the oxide capacitance, and $Q_{ox}$ is the fixed oxide charge. A positive threshold voltage ensures that the device will be normally-off and this can be achieved by varying the doping concentration and thickness of the $N^-$ layer above the buried $P^+$ layer. For a given doping concentration, the maximum thickness, ($t_{n,max}$) of this $N^-$ layer (to get a normally off device) can be derived by setting the condition that the threshold voltage is $\geq 0V$. Using this criterion, we get the following expression for $t_{n,max}$ :

$$t_{n\,max}^2 = \left( V_{bi} + \phi_{ms} - \frac{Q_{ox}}{C_{ox}} \right) \frac{2\varepsilon}{qN_D\left(1 + \frac{N_D}{N_A}\right)} \qquad (2)$$

where $N_D$ and $N_A$ are the donor and acceptor concentrations in the $N^-$ and $P^+$ regions. Thus, the thickness and doping of this $N^-$ layer have to be carefully chosen such that it is completely depleted by the built-in potentials of the $P^+$/ N junction and the MOS gate at zero gate bias, resulting in a normally-off device.

In the ACCUFET structure, when the gate bias is zero, there is no path (channel) for the conduction of electrons from the source to the drain and the entire drain voltage is supported by the reverse biased $P^+$/N-drift junction. Since this $P^+/N^-$ junction can support high voltages [8], the device is expected to have a high breakdown voltage. In the blocking mode of operation, the channel potential barrier created by the built-in potentials of the $P^+/N^-$ junction and the MOS gate prevent any current conduction. In order to prevent the drain potential from encroaching into the channel region and lowering the channel potential barrier, the channel has to be well shielded. This can be achieved by reducing the gap between the two $P^+$ layers ($W_{Jch}$) which results in the merging of the depletion regions from the two $P^+$ layers at a low drain voltage and shielding the channel region from high drain voltages. Decreasing $W_{Jch}$ also helps in reducing the electric field in the gate oxide and the field crowding at the $P^+$ layer edge thereby increasing the breakdown voltage (BV) of the device.

When a positive gate bias is applied, an accumulation channel (of electrons) is created at the $SiO_2$/SiC interface. This results in a low resistance path for the electron current flow from the source to the drain. Assuming that the higher accumulation layer mobility (as compared to the inversion layer mobility) observed in silicon applies to silicon carbide also, a lower on-resistance is expected for the planar ACCUFET. As discussed earlier, decreasing $W_{Jch}$ is expected to reduce the maximum gate oxide electric field and increase the BV. However, when $W_{Jch}$ is decreased, the cross-sectional area for current flow from the channel into the drift region decreases and this will result in an increase in the specific on-resistance of the device as will be explained in the following section.

### *Modeling of On-Resistance*

The on-resistance of the planar ACCUFET is the total resistance between the source and drain terminals in the on-state. The on-resistance is an important device parameter because it determines the maximum current rating and the on-state voltage drop. The total on-resistance of the SiC ACCUFET is given by:

$$R_{on} = R_{on,sc} + R_{on,n^{+}} + R_{on,ch} + R_{on,j} + R_{on,d} + R_{on,s} + R_{on,dc} \tag{3}$$

where $R_{on,sc}$ is the source contact resistance, $R_{on,n}{}^{+}$ is the contribution from the $N^{+}$ source region, $R_{on,ch}$ is the accumulation channel resistance, $R_{on,j}$ is the contribution from the drift region between the two $P^{+}$ layers, $R_{on,d}$ is the drift region resistance, $R_{on,s}$ is the substrate resistance, and $R_{on,dc}$ is the contribution from the drain contact. In a typical high voltage device, the contribution from $R_{on,n}{}^{+}$ is generally negligible due to the high doping and can be ignored.

The accumulation channel resistance is dependent on the charge in the accumulation layer and the mobility of the free carriers at the accumulated surface. The accumulation channel resistance is given by

$$R_{on,ch} = \frac{L_{ch}}{Z\mu_{na}C_{ox}(V_G - V_{ta})} \tag{4}$$

where $L_{ch}$ is the channel length, $\mu_{na}$ is the accumulation channel mobility, Z is the channel width, $V_G$ is the gate voltage and $V_{ta}$ is the threshold voltage of the ACCUFET.

Under the assumption that the voltage drop along the vertical direction in the gap between the two $P^+$ layers is small enough not to change the depletion layer width, the resistance of the JFET region ($R_{on,j}$) can be calculated by finding the undepleted width (*b*) through which the current flows.

$$R_{on,j} = \frac{t_P}{q\mu_n N_D Z b} \tag{5} \text{ ;}$$

$$b = W_{Jch} - 2\sqrt{\frac{2\varepsilon}{qN_D}V_{bi}} \tag{6}$$

where $t_p$ is the thickness of the buried $P^+$ layer, $N_D$ is the epilayer doping concentration, and $\mu_n$ is the electron mobility in the vertical direction.

To analyze the spreading resistance of the drift region ($R_{on,d}$), the drift region is assumed to begin below the bottom of the $P^+$ layer. The current spreads from the JFET region into the drift region. The mobility anisotropy [9] in 6H-SiC leads to excellent current spreading because the mobility in the lateral direction is 4.8X higher than that in the vertical direction. We have found that a reasonably accurate estimation of the drift region spreading resistance can be obtained by assuming that the current spreads from a cross-section of width *b* at an angle given by $\tan^{-1}(4.8)$ (=78.2°). The current flow paths overlap at a depth of $W_P/4.8$ below the $P^+$ layer and the drift region resistance can be modeled as the sum of a region where the cross-section for current flow increases with depth and a second region with uniform cross-section equal to the cell-width, $W_{cell}$. This leads to a drift region spreading resistance given by:

$$R_{on,d} = \frac{1}{9.6 q \mu_n N_D Z} \ln\left[\frac{b + 2W_P}{b}\right] + \frac{\left(t_d - \dfrac{W_P}{4.8}\right)}{q \mu_n N_D Z W_{cell}} \tag{7}$$

where $t_d$ is the thickness of the drift region below the $P^+$ layer and $W_p$ is the width of the buried $P^+$ layer as defined in Fig.1.

The contribution from the $N^+$ substrate is given by:

$$R_{on,s} = \rho_s t_s \tag{8}$$

where $\rho_s$ is the substrate resistivity and $t_s$ is the substrate thickness. For commercial 6H-SiC substrates, the lowest substrate resistivity currently available is about 0.1Ω-cm. The specific substrate resistance for a typical substrate thickness of 300μm, will be 3mΩ-cm$^2$ which forms a significant part of the total device specific resistance of a typical 1000V device. Hence this resistance needs to be reduced by thinning of the substrates or decreasing the substrate resistivity from what is available today.

Typically, the channel resistance and the drift region resistance are the main components that determine the total on-resistance of the device. Normally the specific on-resistance, which is the resistance of a device with unit area is used for comparison of devices. The on-resistance ($R_{on}$) can be converted to specific on-resistance ($R_{on,sp}$) by multiplying it by the area of the device cell ($W_{cell}$.Z) . For a typical ACCUFET device containing a 10μm thick $N^-$ epilayer doped at $10^{16}$ cm$^{-3}$ with a cell pitch of 23 μm, $W_{Jch}$ of 4 μm and a $\mu_{na}$ of 125 cm$^2$/V.s, the calculated (using Eq.3) $R_{on,sp}$ is 18.5 mΩ-cm$^2$ which is about 2.5X that of the ideal (drift region) $R_{on,sp}$ of 7.7 mΩ-cm$^2$. This clearly shows that the proposed device has very low specific on-resistance if the accumulation channel mobility ($\mu_{na}$) is high. In the experimental section, it will be shown that such high $\mu_{na}$ is achievable in fabricated devices.

## III. Device Simulation

Two dimensional numerical simulations were done using *MEDICI* [10] for the ACCUFET structure with a 10μm thick $N^-$ drift region doped at $10^{16}$ $cm^{-3}$. The buried $P^+$ layer had a Gaussian profile located between 0.3μm and 0.7μm with a peak concentration of $5x10^{18}$ $cm^{-3}$. An $N^+$ polysilicon gate electrode with a 100A thick gate oxide ($Q_F = 10^{11}$ $cm^{-2}$) was used. The baseline device had a cell pitch of 23μm and a channel length of about 2.5μm. The spacing between the $P^+$ layers, ($W_{Jch}$) was varied from 2 to 4μm. The simulations predicted a blocking voltage of 1550V and a specific on-resistance of 15-23 mΩ-$cm^2$ for the different values of $W_{Jch}$ as described in Table.1

| $W_{Jch}$ (μm) | Simul. $V_F$ (Volts) ($L_{ch}$=2.5μm) | Simul. BV (Volts) ($L_{ch}$=2.5μm) | Simul. $R_{on,sp}$ (mΩ-$cm^2$) ($L_{ch}$=2.5μm) | Simul. $R_{on,sp}$ (mΩ-$cm^2$) ($L_{ch}$≅7μm) | Analy. $R_{on,sp}$ (mΩ-$cm^2$) ($L_{ch}$≅7μm) | Meas. $R_{on,sp}$ (mΩ-$cm^2$) ($L_{ch}$≅7μm) | Simul. Max. $E_{ox}$ (MV/cm) |
|---|---|---|---|---|---|---|---|
| 2 | 2.80 | 1560 | 26.0 | 33.5 | 32.5 | 35.6±1.5 | 3.3 |
| 3 | 2.05 | 1550 | 20.2 | 26.4 | 26.7 | 28.8±1.2 | 4.3 |
| 4 | 1.85 | 1540 | 18.1 | 22.5 | 23.9 | 26.7±1.1 | 4.8 |

Table.1 Effect of varying the gap in the $P^+$ buried layer ($W_{jch}$) on the various device parameters. The on-state voltage drop ($V_F$) and specific on-resistance ($R_{on,sp}$) were obtained at a gate bias of 4V. The electric field in the gate oxide ($E_{ox}$) is given at a drain bias of 1500V. $\mu_{na}$=120 $cm^2$/V.s was used in simulations and analytical calculations.

From the simulations, it was found that the electric field near the $SiO_2$/SiC interface can be controlled by adjusting $W_{Jch}$. When $W_{Jch}$ is reduced, the depletion layers from the two neighboring P-N junctions merge and the region above it gets shielded from the high drain voltage, reducing the electric field under the oxide. The three-dimensional electric field profile shown in Fig.2 clearly demonstrates that while the peak electric field occurs at the edge of the $P^+$ layer, the electric field at the oxide interface is much less. The electric field in the drift region below the gate oxide (in the region between the two $P^+$ layers) for different $W_{Jch}$ is shown in Fig.3. It can be clearly seen that as $W_{Jch}$ is decreased, the field at the interface decreases. It is worth pointing out that the peak electric field occurs inside the drift region at about y=1.6μm and the electric field is much lower near the $SiO_2$/SiC interface. Simulations predict that with $W_{Jch} \leq$ 4μm, the peak electric field in the gate oxide can be kept below 5 MV/cm (<2 MV/cm in SiC at the interface) even when the maximum electric field in SiC approaches 3 MV/cm. Thus the oxide rupture problem [3] is solved while still enabling utilization of the high breakdown electric field strength of SiC.

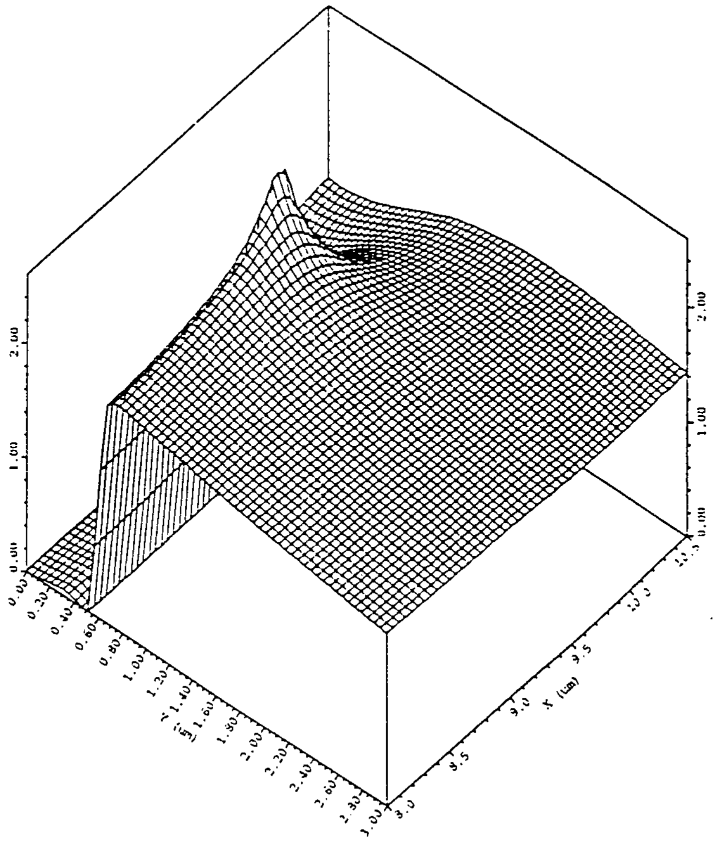

Fig.2 Simulated three-dimensional electric field profile showing the location of the peak electric field and the electric field reduction at the $SiO_2$ /SiC interface.

From the above discussion, it is clear that as $W_{Jch}$ is decreased the maximum electric field in the gate oxide decreases as shown in Table.1. In contrast, it was found that varying $W_{Jch}$ had very little effect on the breakdown voltage, changing it from 1540V to 1560V when $W_{Jch}$ was decreased from 4 to 2μm.This is because even for a $W_{Jch}$ of 4μm, the depletion layer curvature is very small for an epitaxial layer doping concentration of $1x10^{16}$ $cm^{-3}$ resulting in minimal electric field crowding at the junction edge. So reducing $W_{Jch}$ any further will result in only negligible increase in the BV. However, when $W_{Jch}$ is decreased, the forward voltage drop, $V_F$ (at $100A/cm^2$) increases because the current has to now flow through a constricted region. This can be clearly seen in Fig.4 which shows current flow lines in the on-state for two cases of $W_{Jch}$. It may also be noted from this figure that the current spreads rapidly (~80°) once it enters the drift region due to the mobility anisotropy effect which was discussed earlier. The effect of changing $W_{Jch}$ on the $V_F$ is given in Table.1. Thus, there is a trade off between reducing the forward voltage drop by increasing $W_{Jch}$, and reducing the maximum gate oxide field by decreasing $W_{Jch}$. Based on the simulation results, an optimum value for $W_{Jch}$ of 3μm gives a good compromise between obtaining low $V_F$ and $E_{ox}$.

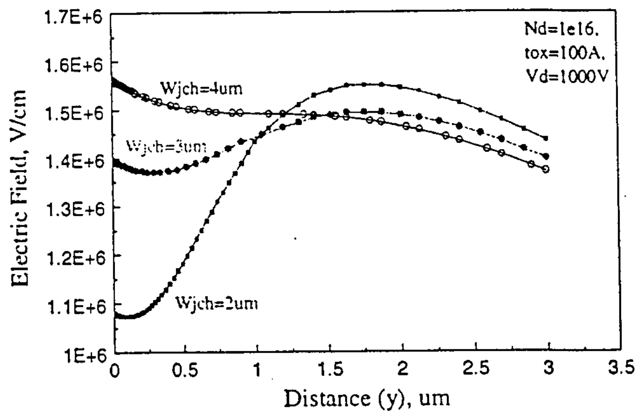

Fig.3 Effect of the size of the gap in the $P^+$ buried layer ($W_{jch}$) on the electric field profile below the gate oxide in the region between the gap in the $P^+$ buried layer. These profiles were obtained at a drain bias of 1000V. The $SiO_2$ /SiC interface is located at y=0.

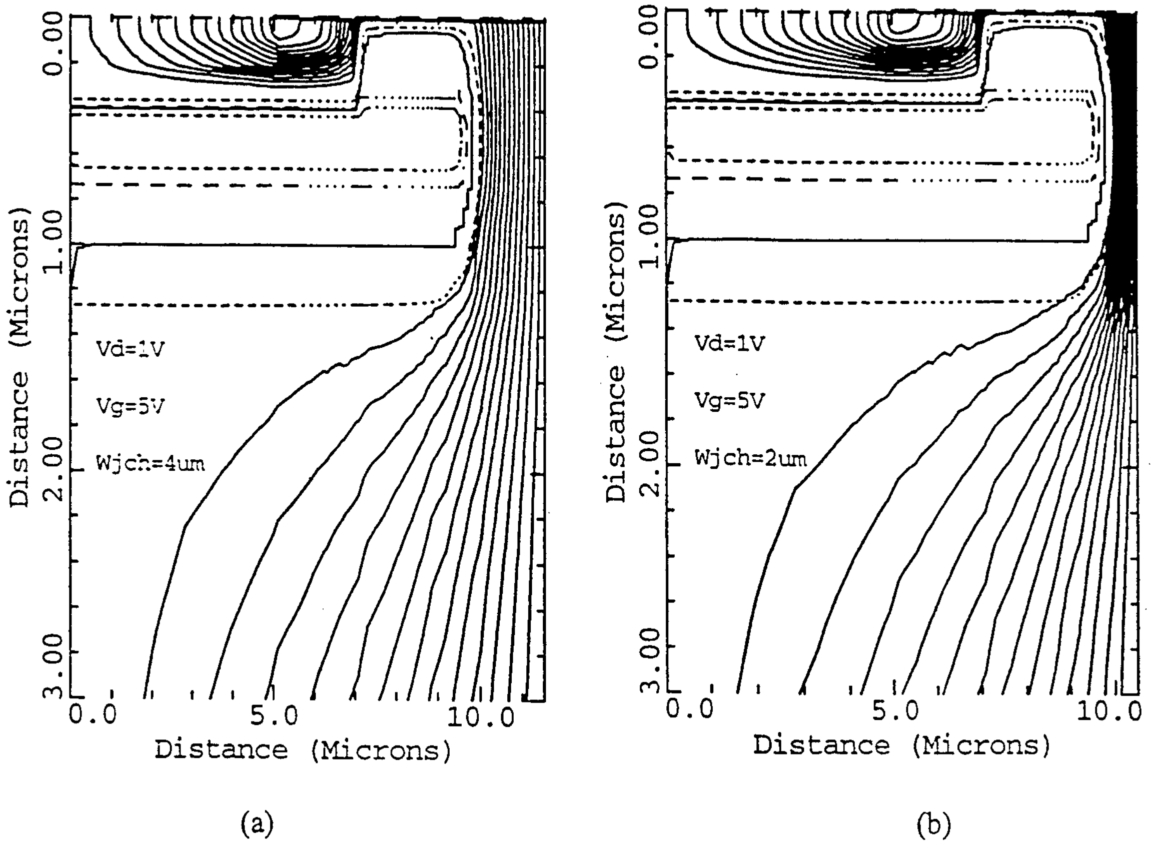

Fig.4 Simulated current flow lines under on-state condition (Vg=5V, Vd=1V) for (a) $W_{Jch}$=4μm, (b) $W_{Jch}$=2μm.

## IV. Device Design and Fabrication

After verifying the concept of the planar SiC ACCUFET through two-dimensional simulations, devices were designed to experimentally demonstrate their operation. The devices were designed with various geometrical cell design parameters with an inter-digitated linear geometry using 2μm design rules. The baseline device had a cell pitch of 23μm with a $W_P^+$ of 19μm. While some designs had metal finger contacts on the $N^+$ source, other designs just had a metal contact on the $N^-$ source pad area. Hence for those devices with remote source contact, the $N^+$ sheet resistance also gets added on to the total device resistance. No termination structure is used for all the devices.

Single crystal N-type ($2x10^{18}$ $cm^{-3}$) 6H-SiC substrates [11] with 10μm thick nitrogen doped ($10^{16}$ $cm^{-3}$) epitaxial layers were used to fabricate the planar ACCUFETs. The buried junction was formed by a single high energy (380 KeV) boron implantation at a dose of $1x10^{14}$ $cm^{-2}$. Monte Carlo simulations using SUPREM III predicted a channel thickness of about 0.3μm and a junction depth of 0.7μm which was confirmed by SIMS measurements. This implant was followed by multiple lower energy boron implants (30,100,200KeV) at the pad area so that contact could be made to the buried layer and at also the periphery to isolate the source from the drift region at the edges of the device. Multiple energy (40,100KeV) nitrogen implants at a dose of $8x10^{14}$ $cm^{-2}$ was used to form the $N^+$ source regions. All implants were annealed at 1400 °C in argon for 30 minutes. After a standard RCA clean, the gate oxide was thermally grown using wet oxidation at 1100 °C followed by re-oxidation at 950 °C to reduce $D_{it}$ and $Q_f$ [12]. A 0.5μm thick polysilicon was deposited by LPCVD and doped with phosphorus at 875 °C. The polysilicon was patterned using $SF_6/O_2$ RIE and isolation oxide was thermally grown on the patterned polysilicon. Ti/Al was used to form both front and back side ohmic contacts [13].

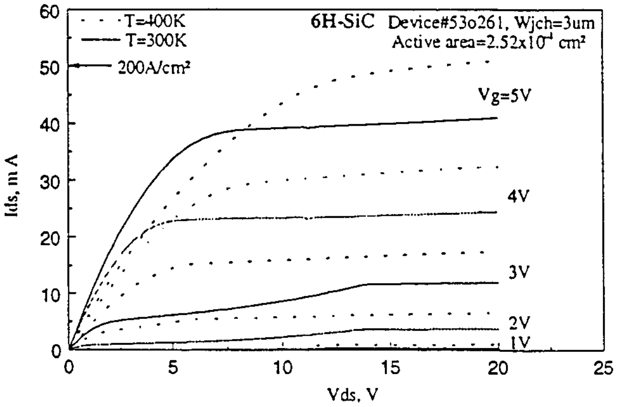

Fig.5 This figure shows the effect of temperature on the measured output characteristics of a typical 6H-SiC ACCUFET

## V. Experimental Results and Discussion

Capacitance -voltage measurements on MOS capacitor test elements gave a gate oxide thickness of 125 A and a fixed oxide charge of ~$10^{12}$ $cm^{-2}$. The $N^+$ source sheet resistance was measured to be 2.2KΩ/sq. at room temperature which is in reasonable agreement with the expected (simulation) value of 1.5KΩ/sq; the slightly higher value is probably due to the incomplete activation of dopants at this annealing temperature.

The buried $P^+$ layer was shorted to the source during all the measurements. Excellent I-V characteristics were obtained on the fabricated planar ACCUFETs with good current saturation and gate control as shown in Fig.5. The unterminated devices had a breakdown voltage (BV) of 350V with a leakage current of <100 μA just before breakdown. There was no deterioration in the BV with repeated measurement on the same device as long as the current at breakdown was limited to 5 mA (20A/$cm^2$). The gate current was monitored during BV measurement and found to be <1nA even during the device breakdown. This demonstrates that the breakdown is non-catastrophic and the gate oxide rupture, which has been a major problem in SiC UMOSFETs [4], is prevented. A room temperature specific on-resistance ($R_{on,sp}$) of 18 mΩ-$cm^2$ was measured on the best device (cell pitch = 21μm, $W_{Jch}$ = 4μm and $L_{ch}$ = 2.5μm) at a gate bias of only 5V. Thus, the fabricated ACCUFETs have excellent on-state conduction even with the low (logic-level) gate voltages. In contrast, most of the previous SiC MOSFETs [4,5,14] have used high voltage (25-60V) gate drive in order to obtain on-state conduction which is usually unacceptable in power electronic systems. It may also be pointed out that the ACCUFET device can carry extremely high currents (>300A/$cm^2$) even when operating at a small gate bias of 5V. Hence these ACCUFETs can be operated at high current densities resulting in smaller device areas, higher yield and lower cost.

The specific on-resistance of this device is much lower than that of the previously reported best 6H-SiC 50V UMOSFET (38 mΩ-cm$^2$) [15] and the best 6H-SiC DIMOSFET (760V, 125 mΩ-cm$^2$) [6]. The calculated specific on-resistance for the drift region in the fabricated ACCUFET devices is 7.7 mΩ-cm$^2$. Thus, the measured specific on-resistance for the planar ACCUFET device is within 2.5X of the drift region which can support over 1500V. We believe that this is the best value obtained so far for any high voltage SiC MOSFET structure.

As mentioned earlier, while some designs had metal finger contacts on the $N^+$ source, other designs just had a metal contact only on the $N^+$ source pad area to reduce the likelihood of gate to source shorts. It was observed that the devices with source metal fingers had low $R_{on,sp}$ , typically < 25 mΩ-cm$^2$ whereas those with remote source contacts had higher $R_{on,sp}$ , in the range of 200 mΩ-cm$^2$. This was expected because for those devices with remote source contact, the $N^+$ sheet resistance (which is high) gets added on to the total device resistance. The effect of this high sheet resistance can be accounted for by modeling the current flow through the $N^+$ source finger in the z-direction. The voltage along the $N^+$ source finger will increase as z increases. An expression for this voltage V(z) can be derived under the following assumptions: (i) The $N^+$ source finger sheet resistance is uniform, (ii) $V_{DS} << V_{GS}$ (true in the on-state) and therefore the MOS channel resistance remains constant, (iii) the drift region resistance is constant.

$$V(z) = V_{DS}(1 - e^{-kz}) \tag{9}$$

where $k = \sqrt{\dfrac{R_{sh}}{W_{N^+} R_{dev}}}$ (10)

where $R_{sh}$ is the $N^+$ source finger sheet resistance, $W_N{}^+$ is the width of the $N^+$ source finger, and $R_{dev}$ is the device resistance per unit length for $R_{sh}$=0. This expression is derived under the assumption that $k.L_{N}^{+}$ is large ($e^{-kL_{n}^{+}} \cong 0$), where $L_{N}^{+}$ is the length of the $N^{+}$ source finger. Using this equation, the ratio of the total specific on-resistance with and without $R_{sh}$ is given by

$$\frac{R_{on,\,sp}(R_{sh} \neq 0)}{R_{on,\,sp}(R_{sh} = 0)} = kL_{N^{+}} \tag{11}$$

For a typical device with $R_{sh}$=2.2KΩ/sq., $W_{N}^{+}$ =6.5μm, and $L_{N}^{+}$ =150 μm, we get $k.L_{N}^{+}$ = 9.5. This means that the devices with out source metal fingers will have 9.5 times higher $R_{on,sp}$ than identical devices with source metal fingers. This is consistent with the values of ~20 mΩ-cm$^{2}$ and ~200 mΩ-cm$^{2}$ measured for the devices with and without metal fingers.

Measurements were done on devices with different $W_{Jch}$ and specific on-resistances ($R_{on,sp}$) was determined. Since these devices had only remote source contact, the correction factor ($k.L_{N}^{+}$) was used in extracting the $R_{on,sp}$. It was observed that as $W_{Jch}$ was increased, $R_{on,sp}$ decreased as expected. The measured specific on-resistances for the different $W_{Jch}$ along with the simulated and analytically calculated values are given in Table.1. In the simulations and analytical calculations, the contribution from the substrate resistance was neglected. This was done because in the measured devices, the effective substrate resistance is very small (<5% of the usual $R_{on,s}$ ) due to wafer level probing which leads to current spreading in the substrate. It may be noted although the measured value is slightly higher, possibly due to contributions from the contact resistances, there is good agreement between these values.

The threshold voltage $V_{ta}$ and the accumulation channel mobility $\mu_{na}$ was extracted from the transfer characteristics shown in Fig.6. The intercept on the X-axis of this plot gives the threshold voltage which was extracted to be +0.76V at room temperature (300K). From the slope of this plot, the effective room temperature accumulation channel mobility was calculated to be 120 cm$^{2}$/V-s. It is worth pointing out that this value is higher than the highest reported inversion layer mobility (72 cm$^{2}$/V-s) in lateral 6H-SiC MOSFETs [12] and much higher than values obtained in vertical power device structures [4-6] leading to low specific on-resistance for the ACCUFET.

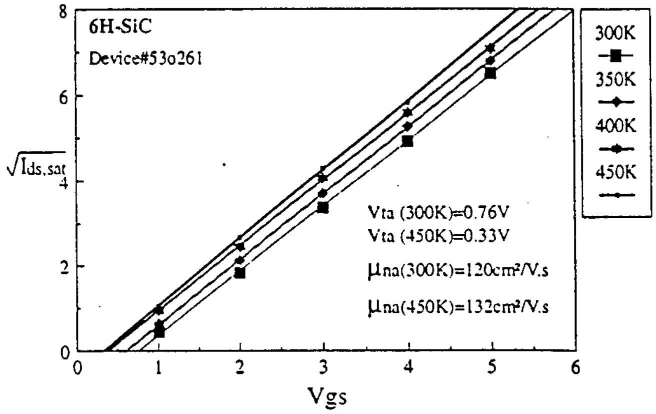

Fig.6 Measured transfer characteristics of a typical device for different temperatures.

### *High Temperature Characteristics*

The devices were characterized at elevated temperatures (up to 450K) to observe the effect of temperature on the device performance. It can be seen from the high temperature output characteristics shown in Fig.5 that both the on-resistance and the saturation current increases with temperature.

The dependence of the threshold voltage on temperature was also measured. As expected, the $V_T$ decreases from 0.76 V at room temperature to 0.33V at 450K (~ -3 mV/°C) as can be seen from the Fig.6. The effective accumulation channel mobility extracted from the plot increased slightly from 120 to 132 $cm^2$/V-s when the temperature was increased from 300K to 450K. However, on a similar device, the accumulation channel mobility decreased slightly from 125 to

120 $cm^2/V$-s for the same temperature range. These changes are too small and fall within the measurement and extraction error and hence no definitive trend in the effective accumulation channel mobility with temperature could be obtained. So it may be concluded that the accumulation channel mobility in these devices remains almost independent of temperature, unlike inversion layer mobility which increases rapidly with temperature [16] giving rise to the undesirable negative temperature coefficient of on-resistance for the inversion channel power devices reported in the literature [5].

The variation of the specific on-resistance as a function of temperature (300-450K) was measured. It was seen that while some devices showed an increase in $R_{on,sp}$ with temperature, some showed a slight decrease with temperature as shown in Fig.7. Analysis of the design variations of these devices showed that all the devices which had source metal fingers (and hence low $R_{on,sp}$) exhibited a positive temperature coefficient whereas those which had remote source contacts showed a negative temperature coefficient. The $R_{on,sp}$ of the devices with source metal fingers had a temperature dependence of $T^n$ where $n$ varied from 1.4 to 1.73 for the different devices. Measurements on test elements show that the drift region also has a positive temperature coefficient as shown in Fig.7 with an $n$ value of 1.82 which is consistent with published values [17]. Although the electron mobility in 6H-SiC varies as $T^{-n}$ where n=2.5 [18], the $R_{on,sp}$ does not increase with an $n$ value of 2.5 because of the increase in the carrier concentration due to the improved dopant ionization at higher temperatures. If the total on-resistance of the device was composed of only the drift region resistance, the device also would have an $n$ of 1.82. However, the total device resistance consists of other components such as the channel, contact, substrate resistance etc. (Eq.3) and the fact that the device resistance had an $n < 1.82$ shows that these components collectively have a lower ($n<1.82$) temperature dependence. The most important point to be noted is that these devices have a strong positive temperature coefficient unlike previous SiC MOSFETs [5]. A positive temperature coefficient is extremely desirable since it allows paralleling of devices and also improves reliability by avoiding current filamentation problems.

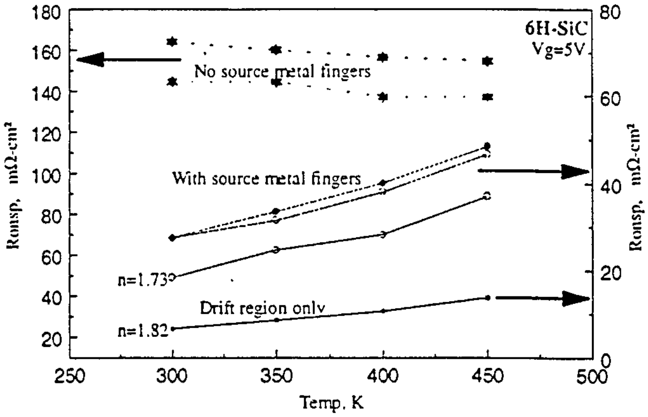

Fig.7 Specific on-resistance for the two sets of devices and that of the drift region measured as a function of temperature.

As mentioned earlier, the devices with remote source contact had a slight negative temperature coefficient. It is possible to get a negative temperature coefficient only if one of the components have a negative temperature coefficient. The $N^+$ source sheet resistance was measured as a function of temperature and it was revealed to have a negative temperature coefficient with an $n$ value of -1.25 resulting in a negative temperature coefficient for the total specific on-resistance for these devices.

## VI. Conclusions

In this paper, the characteristics of the planar 6H-SiC ACCUFET have been analyzed. Two-dimensional numerical simulations show that this structure does not suffer from the gate oxide rupture problem prevalent in SiC UMOSFETs and also has a low specific on-resistance (2X of ideal). Simulations show that the maximum electric field in the gate oxide can be reduced by decreasing the gap between the $P^+$ buried layers ($W_{Jch}$), but at the expense of an increase in the specific on-resistance. The fabricated devices had extremely good current saturation and low measured specific on-resistance of 18 mΩ-cm$^2$ at a gate bias of only 5V. A high accumulation channel mobility of about 120 cm$^2$/V.s was experimentally measured on the fabricated devices. Due to the high channel conductance and low specific on-resistances, these ACCUFETs can be operated at high current densities resulting in smaller device areas, higher yield and lower cost. The simulations predicted a decrease in the specific on-resistance with increasing gap between the $P^+$ buried layers ($W_{Jch}$) which was confirmed by experimental results. The specific on-resistance was demonstrated to have a positive temperature coefficient which is highly desirable for power devices.

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# A Planar Lateral Channel SiC Vertical High Power JFET

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***Abstract:*** This paper describes a novel planar lateral channel SiC high power JFET structure. Two-dimensional numerical simulations predict low on-resistances with excellent current saturation and square FBSOA which have been experimentally confirmed. The fabricated 6H-SiC devices had a low specific on-resistance of 9 mΩ-cm$^2$ at room temperature for a channel dose of $2x10^{13}$ cm$^{-2}$. This measured specific on-resistance is within 3X of the value calculated for the epitaxial drift region ($2.5x10^{16}$ cm$^{-3}$, 10μm ). The 4H-SiC JFETs had excellent current saturation up to 1100V even at current densities as high as 250A/cm$^2$.

***Introduction:*** Silicon carbide power MOSFETs with the UMOS structure have been recently reported [1-4]. These UMOSFETs suffer from two serious problems: (i) the high electric field at the trench corners causes destructive breakdown of the gate oxide at high drain voltages, and (ii) the extremely low inversion layer mobility [5] results in a higher specific on-resistance, nullifying the advantage of low drift region resistance in SiC. In the trench UMESFET structure [6], the low inversion layer mobility problem is eliminated, but this structure still suffers from the high electric fields at the sharp trench corners. Further, it requires a sophisticated process to achieve gate to source isolation in addition to high resolution lithography to allow channel pinch off with reasonable gate voltages. SiC lateral JFETs with buried gate contact have been reported by various groups [7-9]. These JFETs have low breakdown voltages (<100V) and have high specific on-resistances due to the lack of vertical current flow in these devices. Hence there is a need to consider alternate SiC FET structures. In this paper, we propose and demonstrate a new planar lateral channel, vertical SiC JFET structure with low on-resistance.

***Device Structure and Simulations:*** The schematic cross-section of the proposed device is shown in Fig.1. A lateral channel is formed between the buried $P^+$ layer and the shallow $P^+$ surface gate. The thickness and doping of the channel region can be adjusted to create either a normally-on or -off device. The normally-on device is preferred as it will have a lower on-resistance. When a positive voltage is applied to the drain with the gate at zero bias, current flows from the drain through the gap in the buried $P^+$ layer and then through the channel to the source . The current flow can be modulated by applying a negative gate bias to deplete the channel region. If a sufficient negative bias is applied to the gate to pinch off the channel, a potential barrier is established for the flow of electrons from

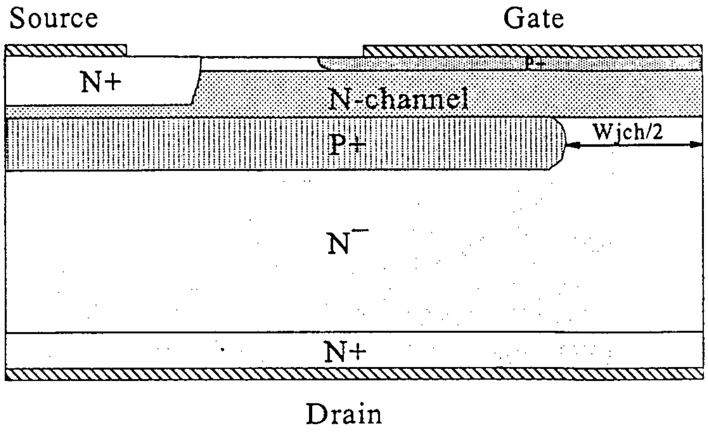

Fig.1 Schematic cross-section of the planar lateral channel SiC vertical JFET.

source to the drain. If the barrier is sufficient enough to stop the electron flow, then no current will flow even if the drain bias is increased until we reach the avalanche breakdown voltage. In order to prevent the drain potential from encroaching into the channel region and lowering the channel potential barrier, the channel has to be well shielded. This can be achieved by reducing the gap between the two $P^+$ layers ($W_{Jch}$) which also helps in reducing the electric field crowding at the $P^+$ layer edge thereby increasing the breakdown voltage of the device.

Two dimensional numerical simulations of the vertical JFET structure with a 10 μm thick 6H-SiC epitaxial layer with doping concentration of $2x10^{16}$ $cm^{-3}$ were done using *MEDICI* [10]. Since the maximum energy chosen for the P-type boron implant was 400 KeV, the maximum channel thickness is only 0.35μm. This channel thickness is fully pinched off due to the built-in junction potentials if the channel doping is same as the epitaxial layer ($2x10^{16}$ $cm^{-3}$). In order to make a normally-on device, an N-type channel implant is required. Simulations were done with different N-channel implant doses ranging from $1x10^{12}$ to $2x10^{13}$ $cm^{-2}$. The simulated current flow lines for such a device (N-channel dose=$2x10^{12}$ $cm^{-2}$) is shown in Fig.2. From the figure it can be seen that the current spreads rapidly in the drift region giving rise to a uniform current flow in the drift region, thus reducing the on-resistance. The current spreads much faster than a 45 degree angle due to the anisotropy of the mobility in 6H-SiC. In 6H-SiC, the lateral (perpendicular to the c-axis) mobility is about 5 times higher than the vertical mobility. This actually helps us in this device as the biggest contribution to the resistance comes from the channel which is lateral and therefore has 5 times less resistance.

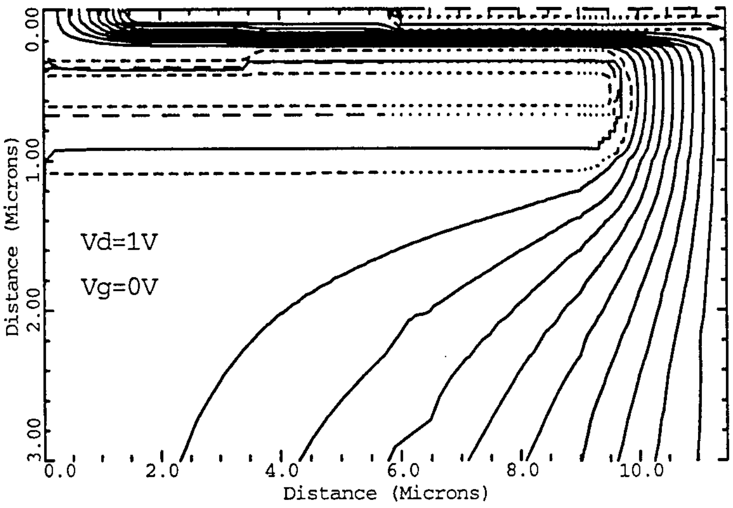

Fig.2 Simulated current flow lines in the planar 6H-SiC JFET at Vds=1V, Vgs=0V.

The simulated on-state and blocking characteristics are shown in Fig.3 and Fig.4 respectively. It may be noted that the device has low on-resistance and linear on-state characteristics even at high current densities due to the low channel resistance. It can be seen from Fig.5 that the potential contours are almost flat and that the field crowding at the $P^+$ layer edge is minimal giving rise to near ideal breakdown voltage. From the blocking characteristics, it may be noted that the device has a high breakdown voltage of about 1025V and 960V for $W_{Jch}$=2 and 4µm respectively.

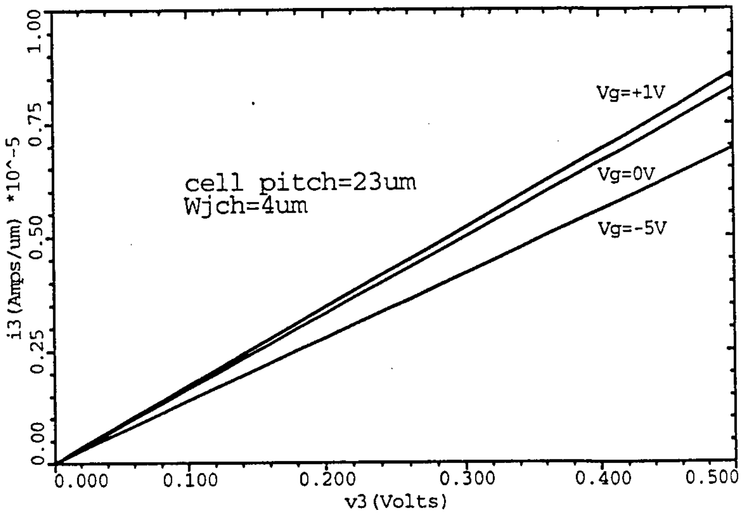

Fig.3 Simulated on-state I-V characteristics of the 6H-SiC JFET structure. (Dose=1e13/$cm^2$, Wjch=4 um)

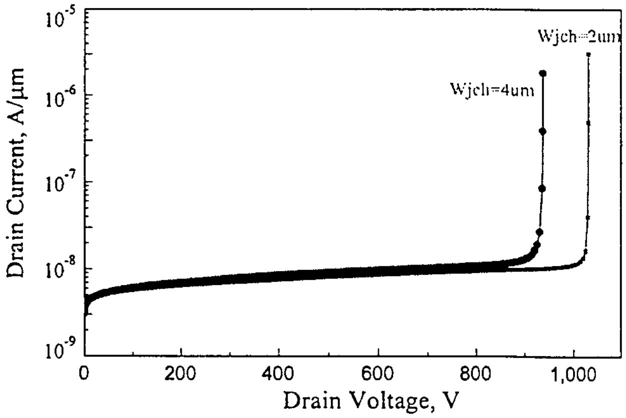

Fig.4 Simulated blocking characteristics of the planar 6H-SiC JFET structure.

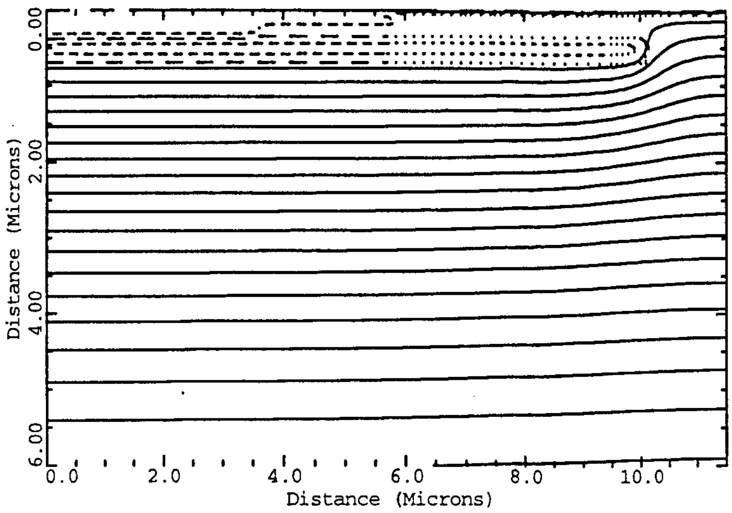

Fig.5 Simulated potential contours at a drain bias of 900V showing minimal electric field crowding at the buried junction edge in the planar 6H-SiC JFET structure.

As expected, the specific on-resistance ($R_{on,sp}$) decreased with increase in the dose as shown in Table.1 for 6H-SiC JFETs. A similar trend was observed for 4H-SiC devices also. The breakdown voltage remains almost constant for low values of channel doses but decreases as the channel dose is increased beyond $2x10^{12}$ $cm^{-2}$. For a given N-channel dose, the $R_{on,sp}$ also decreased with increase in the $P^{+}$ layer spacing ($W_{Jch}$) for both 6H- and 4H-SiC JFETs. However the breakdown voltage decreased slightly with increasing $W_{Jch}$ due to higher electric field at the corner of the buried $P^{+}$ layer. Thus there is a trade-off between reducing the $R_{on,sp}$ and increasing the breakdown voltage by varying $W_{Jch}$.

| W cell μm | W jch μm | Channel implant Dose /cm² x 10¹² | Ron,sp mOhm-cm² | BV Volts |
|---|---|---|---|---|
| 23 | 4 | 1.0 | 28.7 | 957 |
| 23 | 4 | 1.4 | 19.1 | 955 |
| 23 | 4 | 2.0 | 13.8 | 948 |
| 23 | 4 | 10 | 7.0 | 901 |
| | | | | |
| 21 | 2 | 1.0 | 28.9 | 1023 |
| 21 | 2 | 1.4 | 20.5 | 1022 |
| 21 | 2 | 2.0 | 15.4 | 1018 |
| 21 | 2 | 10 | 9.3 | 962 |

Table.1 Effect of N-channel dose and W jch on the 6H-SiC JFET parameters

***Device Fabrication:*** The devices were fabricated on both 6H- and 4H-SiC with 10μm thick N-type homo-epitaxial layers grown on $N^+$ substrates. The epilayer doping concentration was $2.5 \times 10^{16}$ cm$^{-3}$ for 6H-SiC and $1.6 \times 10^{16}$ cm$^{-3}$ for 4H-SiC. A 9 mask process with 2μm design rule was used. The buried $P^+$ layer was formed by boron implantation at 380 KeV (dose=$1 \times 10^{14}$ cm$^{-2}$) followed by multiple lower energy boron implants at the pad area so that contact could be made to the buried layer. A shallow 10 KeV boron implant (dose=$1 \times 10^{15}$ cm$^{-2}$) was used to form the upper $P^+$ gate region. The $N^+$ source regions were formed by nitrogen implantation (40,100KeV, $8 \times 10^{14}$ cm$^{-2}$). Three different N-channel doses of $1 \times 10^{12}$, $1 \times 10^{13}$ and $2 \times 10^{13}$ cm$^{-2}$ were used to study the effect of N-channel dose on the device characteristics. All implants were annealed at 1400 °C in argon for 30 minutes. Al ohmic contacts were made to the $P^+$ regions using RTA at 900 °C for 60 sec. Ti/Al was used for ohmic contacts to the $N^+$ source and drain regions.

***Experimental Results:*** All the devices were characterized using a computerized Keithley model 251 system at room temperature. All the JFETs except those which received $10^{12}$ cm$^{-2}$ dose N-channel implant exhibited pentode-like characteristics with excellent on-resistance and good saturation characteristics. The devices with $1 \times 10^{12}$ cm$^{-2}$ dose N-channel implant were normally-off and had very high on-resistance due to the absence of a conducting channel. The on-state performance of these devices could not be improved even by applying a positive gate bias since the maximum positive gate bias was limited to about 3V, beyond which the gate current increases rapidly. Hence only the results obtained on the $1 \times 10^{13}$ and $2 \times 10^{13}$ cm$^{-2}$ dose devices are reported below. Since the devices on 6H-SiC and 4H-SiC had different characteristics, they are discussed separately.

***6H-SiC JFETs:*** The on-state I-V characteristics of two typical 6H-SiC devices which received the different doses of N-channel implants are shown in Fig.6 (a) and (b). It can be seen that the devices are normally-on with very good conduction at zero gate bias. They had excellent specific on-resistance of 11 mΩ-cm$^2$ for channel dose of 1x10$^{13}$ cm$^{-2}$ and 9 mΩ-cm$^2$ for channel dose of 2x10$^{13}$ cm$^{-2}$. These measured values come close to the specific on-resistances obtained from simulation of 7 mΩ-cm$^2$ for a dose of 1x10$^{13}$ cm$^{-2}$ and 6.3 mΩ-cm$^2$ for 2x10$^{13}$ cm$^{-2}$ . It is worth pointing that the ideal $R_{on,sp}$ is 3.2 mΩ-cm$^2$ (for 10μm, 2.5x10$^{16}$ cm$^{-3}$ doped epilayer) and hence these fabricated devices have specific on-resistances within 3X of the ideal value. The gate bias could modulate the drain current well by pinching off the channel for the devices which received a channel dose of 1x10$^{13}$ cm$^{-2}$. However, the gate bias had only little control over the drain current on those which received a channel dose of 2x10$^{13}$ cm$^{-2}$ due to the higher channel doping.

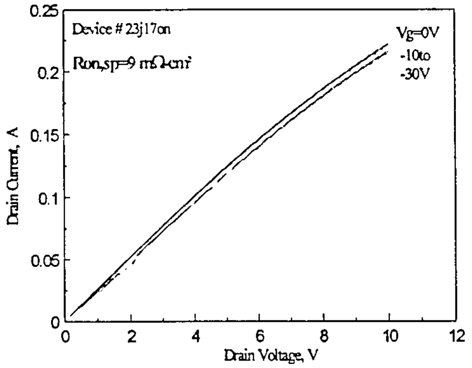

Fig.6 (b) Measured on-state I-V characteristics of the 6H-SiC JFET (dose=2e13/cm²)

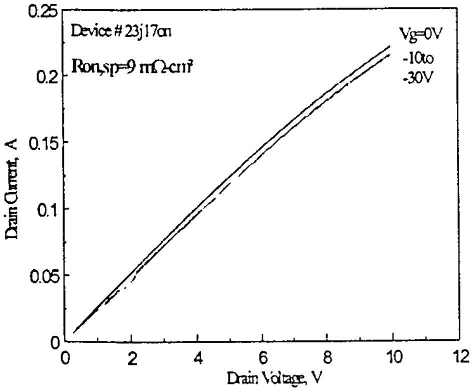

Fig.6 (b) Measured on-state I-V characteristics of the 6H-SiC JFET (dose=2e13/cm²)

The output characteristics of the $1\times10^{13}$ and $2\times10^{13}$ cm$^{-2}$ dose devices are shown in Fig.7 (a) and (b). The devices had low on-resistance followed by excellent saturation as predicted by simulations. It may be pointed out that though the devices with lower channel doping showed better gate control, they could not be taken to the blocking mode because the gate to source junction breaks down at about -60V due to the high channel doping.

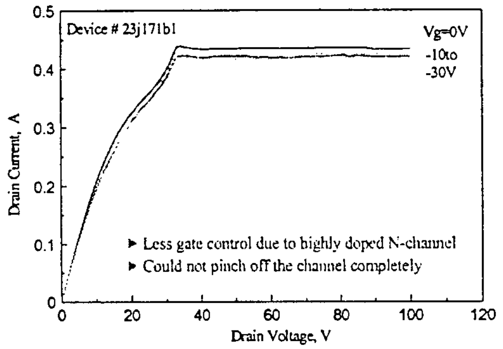

Fig.7 (b) Measured output characteristics of the 6H-SiC JFET (dose=2e13/cm²)

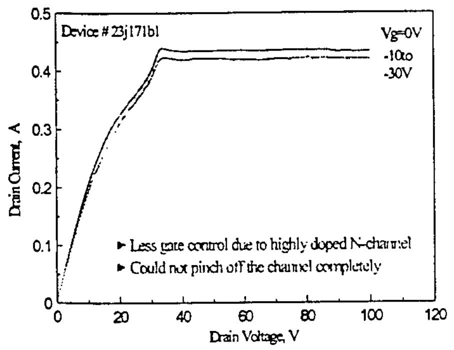

Fig.7 (b) Measured output characteristics of the 6H-SiC JFET (dose=2e13/cm²)

***4H-SiC JFETs:*** The on-state I-V characteristics of two typical 4H-SiC devices which received the two different implants are shown in Fig.8 (a) and (b). They had low specific on-resistance of 14 mΩ-cm$^2$ for channel dose of $1\times10^{13}$ cm$^{-2}$ and 11 mΩ-cm$^2$ for channel dose of $2\times10^{13}$ cm$^{-2}$. Calculations show that the ideal $R_{on,sp}$ is 0.42 mΩ-cm$^2$ (for 10μm, $1.6\times10^{16}$ cm$^{-3}$ doped epilayer) and hence the specific on-resistance of the fabricated devices is much higher (~30X) than the ideal value. The 4H-SiC JFETs exhibited better gate control for both N-channel implant doses when compared with the 6H-SiC devices.

Figures 9 (a) & (b) shows the output characteristics of both the $1\times10^{13}$ and $2\times10^{13}$ $cm^{-2}$ dose devices. The devices had low on-resistance followed by excellent current saturation characteristics. For one device which received a channel dose of $1\times10^{13}$ $cm^{-2}$, the saturation current was below 100mA (the maximum limit on the high voltage measurement equipment) and therefore the drain voltage could be increased up to 1100V. It can be seen from the output characteristics (Fig.9(a)) that the device had excellent saturation up to 1100V indicating a wide FBSOA. It may be pointed out that though the devices had the expected characteristics with good gate control, they could not be taken

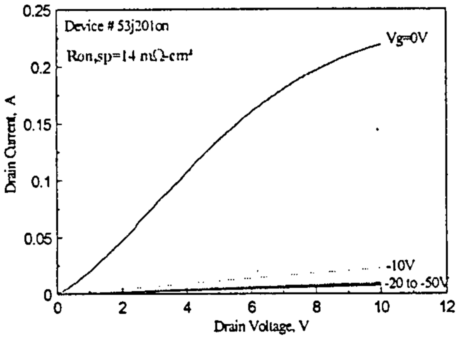

Fig.8 (a) Measured on-state I-V characteristics of the 4H-SiC JFET (dose=1e13/cm²)

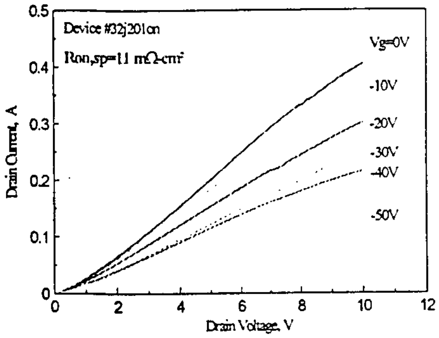

Fig.8 (b) Measured on-state I-V characteristics of the 4H-SiC JFET (dose=2e13/cm²)

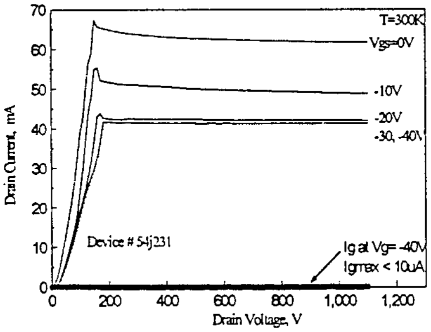

Fig.9 (a). Measured output characteristics of the JFET fabricated on 4H-SiC showing excellent current saturation with BV>1100V.

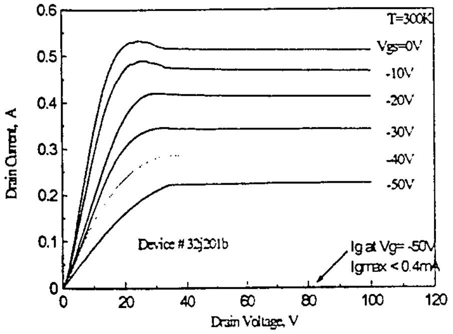

Fig.9 (b) Measured output characteristics of the 4H-SiC JFET (dose=2e13/cm²) to the blocking mode because the gate to source junction breaks down at about 50-60V due to the high channel doping.

***Conclusions:*** Planar high voltage lateral channel vertical SiC JFET devices with low specific on-resistances (within 3X of ideal) were proposed and experimentally demonstrated. It may be pointed out that the on-resistance decreased with increasing N-channel dose for both 6H- and 4H-SiC. Excellent current saturation up to 1100V was measured at current densities as high as 250A/cm$^2$ on 4H-SiC JFETs. These devices may be of interest as high voltage current limiters. Even though the devices had good on-state and saturation characteristics, they could not be completely pinched off due to premature breakdown of the gate junction at about 50V. By comparing the characteristics of the devices with the different doses, it is evident that the lowest dose device had poor on-state characteristics whereas the higher dose devices had poor blocking characteristics. Hence a dose lower than $10^{13}$ cm$^{-2}$ but higher than $10^{12}$ cm$^{-2}$ should give us the best compromise between on-state and blocking characteristics.

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# The Planar Lateral Channel MESFET- A New SiC Vertical Power Device

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***Abstract:*** A novel planar lateral channel SiC MESFET structure with vertical current flow in the drift region is proposed and demonstrated by modeling and fabrication. The normally-on devices fabricated with high channel implant doses had a low room temperature specific on-resistance of 13 m$\Omega$-cm$^2$ and 11.2 m$\Omega$-cm$^2$ for 6H-SiC and 4H-SiC MESFETs, respectively but poor breakdown voltage (~15V). The normally-off devices fabricated with low channel doses had high breakdown voltage (~500V), but poor on-state resistance.

***Introduction:*** The specific on-resistance of silicon carbide power FETs have been projected to be far superior to their silicon counterparts due to the high breakdown field strength of SiC [1]. Most of the research on silicon carbide power switches has been focused on the UMOSFET structure due to the inability to form diffused junctions in SiC. These UMOSFETs suffer from two serious problems: (i) the high electric field at the trench corners causes destructive breakdown of the gate oxide at high drain voltages, [2] and (ii) the extremely low inversion layer mobility [3] results in a higher specific on-resistance, nullifying the advantage of low drift region resistance in SiC. Recently, high voltage 4H-SiC UMOSFETs were reported [4] which can block up to 1100V (<40% of ideal $BV_{pp}$). However, due to low inversion channel mobility (1.5 $cm^2/V.s$), these devices had very high specific on-resistance of 433 $m\Omega$-$cm^2$ (at 300K) which is 125 times higher than the ideal calculated epilayer specific on-resistance. The problems of high electric field in the gate oxide and the low channel (inversion layer) mobility have not been fully addressed in this device. A device that eliminates the low inversion layer mobility problem is the trench UMESFET structure, [5] but this structure still suffers from the high electric fields at the sharp trench corners. Further, it requires a sophisticated process to achieve gate to source isolation in addition to high resolution lithography to allow channel pinch off with reasonable gate voltages. Hence there is a need to create alternate SiC FET structures. In this paper, we propose and demonstrate a new planar lateral channel, vertical SiC MESFET structure.

***Device Structure and Simulations:*** The schematic cross-section of the proposed device is shown in Fig.1. A lateral channel is formed between the buried $P^+$ layer and Schottky gate on the top surface. The thickness and doping of the channel region can be adjusted to create either a normally-on or -off device. The normally-on device is preferred as it will have a lower on-resistance. When a positive voltage is applied to the drain with the gate at zero bias, current flows from the drain through the gap in the buried $P^+$ layer and then through the channel to the source. The current flow can be modulated by applying a negative gate bias to deplete the channel region. If a sufficient negative bias is applied to the gate to pinch off the channel, a potential barrier is established for the flow of electrons from source to the drain. If the barrier is sufficient enough to stop the electron flow, then no current will flow even if the drain bias is increased until we reach the avalanche breakdown voltage. In order to prevent the drain potential from encroaching in to the channel region and lowering the channel potential barrier, the channel has to be well shielded. This can be achieved by reducing the gap between the two $P^+$ layers ($W_{Jch}$) which also helps in reducing the electric field crowding at the $P^+$ layer edge thereby increasing the breakdown voltage of the device.

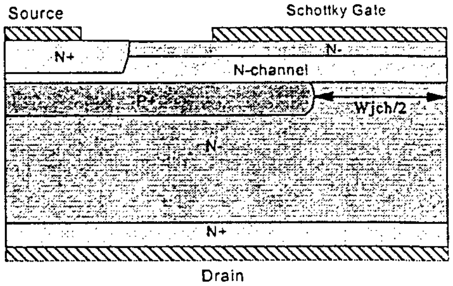

Fig.1 Schematic cross-section of the lateral channel vertical MESFET.

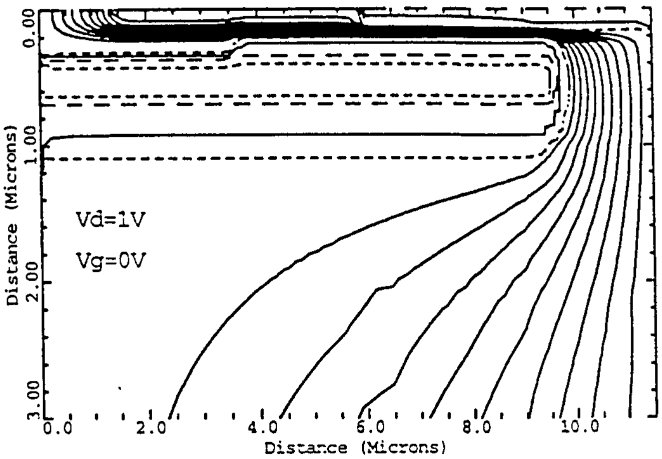

Fig.2 On-state current flow lines in the 6H-SiC MESFET structure. Vg=0V, Vd=1V.

Two dimensional numerical simulations of the vertical MESFET structure with a 10 μm thick 6H-SiC epitaxial layer ($N_D$=2x$10^{16}$ $cm^{-3}$) were done using *MEDICI.* Since the maximum energy chosen for the P-type boron implant was 400 KeV, the maximum channel thickness is only 0.35μm. This channel thickness is fully pinched off due to the built-in junction potentials if the channel doping is the same as the epitaxial layer (2x$10^{16}$ $cm^{-3}$). In order to make a normally-on device, an N-type channel implant is required. Simulations were done with different N-channel implant doses ranging from 1x$10^{12}$ to 2x$10^{13}$ $cm^{-2}$. The simulated current flow lines for such a device (dose = 2x$10^{12}$ $cm^{-2}$) are shown in Fig.2. From the figure, it can be seen that the current spreads rapidly in the drift region giving rise to a uniform current flow in the drift region, thus reducing the on-resistance. The current spreads much faster than the usual 45 degree angle due to the anisotropy of the mobility in 6H-SiC. In 6H-SiC, the lateral (perpendicular to the c-axis) mobility is about 5 times higher than the vertical mobility. This actually helps us in this device as the biggest contribution to the resistance comes from the channel which is lateral and therefore has 5 times less resistance.

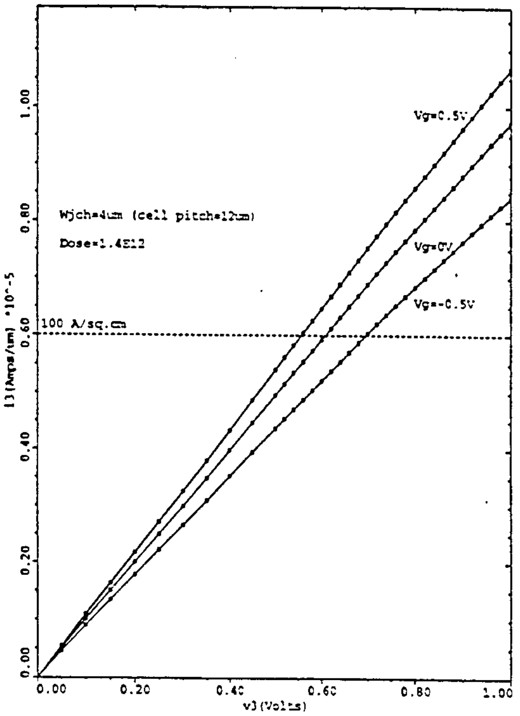

Fig.3 Simulated on-state I-V characteristics of the 6H-SiC MESFET structure. (Dose=1.4e12/cm² , Wjch= 4um)

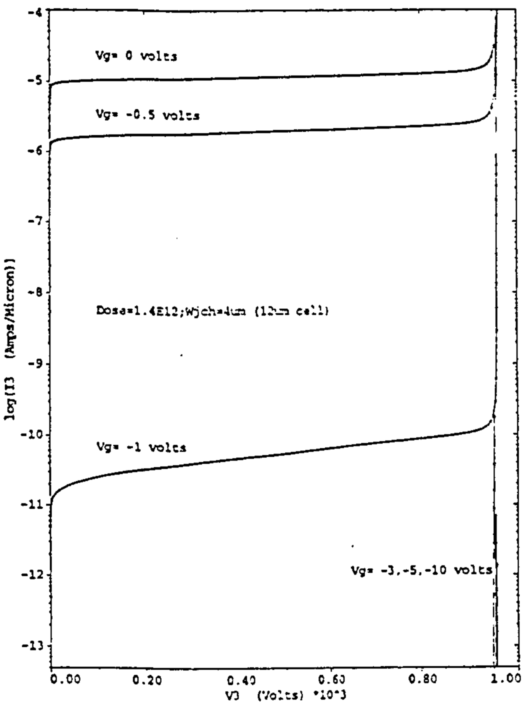

Fig.4 Simulated output characteristics of the 6H-SiC MESFET structure. (Dose=1.4e12/cm² , Wjch= 4um)

The simulated on-state and output characteristics are shown in Fig.3 and Fig.4 respectively. It may be noted that the device has low on-resistance and linear on-state characteristics even at high current densities due to the low channel resistance. From the output characteristics, it may be noted that the device has a high breakdown voltage of about 955V and a square FBSOA which is highly desirable for a power device.

| Wcell μm | Wjch μm | Channel implant Dose /cm² | Ron,sp mOhm-cm² | BV Volts |
|---|---|---|---|---|
| 23 | 4 | 1E12 | 23.9 | 957 |
| 23 | 4 | 1.4E12 | 16.3 | 955 |
| 23 | 4 | 2E12 | 12.5 | 948 |
| 23 | 4 | 1E13 | 6.8 | 901 |
| | | | | |
| 21 | 2 | 1E12 | 24.0 | 1023 |
| 21 | 2 | 1.4E12 | 17.6 | 1022 |
| 21 | 2 | 2E12 | 14.1 | 1018 |
| 21 | 2 | 1E13 | 9.0 | 962 |

Table.1 Effect of N-channel dose and Wjch on the 6H-SiC MESFET parameters

As expected, the specific on-resistance ($R_{on,sp}$) decreased with increase in the channel implant dose as shown in Table.1 for 6H-SiC MESFETs. Due to higher electron mobility, 4H-SiC devices had lower (~3X) specific on-resistance than their 6H-SiC counterparts (4mΩ-cm$^2$ versus 12.5mΩ-cm$^2$ for a channel dose of 2x10$^{12}$ cm$^{-2}$). As the channel dose is increased, the gate voltage required to pinch off the channel also increases, for example - a -10V bias is sufficient for a 2x10$^{12}$ cm$^{-2}$ dose whereas a -50V gate bias is required when the dose is at 2x10$^{13}$ cm$^{-2}$. The breakdown voltage remains almost constant for low values of channel doses but decreases as the channel dose is increased beyond 2x10$^{12}$ cm$^{-2}$. For a given N-channel dose, the $R_{on,sp}$ also decreased with increase in the P$^+$ layer spacing ($W_{Jch}$) for both 6H- and 4H-SiC devices. However the breakdown voltage decreased slightly with increasing $W_{Jch}$ due to higher electric field at the corner of the buried P$^+$ layer. The simulated devices had good blocking characteristics with a breakdown voltage of about 1020V and 955V for $W_{Jch}$=2 and 4μm, respectively.

Thus, there is a trade-off between reducing the specific on-resistance and increasing the breakdown voltage by varying $W_{Jch}$.

***Device Fabrication:*** The devices were fabricated on both 6H- and 4H-SiC with 10μm thick N-type homo-epitaxial layers grown on $N^+$ substrates. The epilayer doping concentration was $2.5\times10^{16}$ $cm^{-3}$ for 6H-SiC and $1.6\times10^{16}$ $cm^{-3}$ for 4H-SiC. An 8 mask process with 2μm design rule was used. The buried $P^+$ layer was formed by boron implantation at 380 KeV followed by multiple lower energy boron implants at the pad area so that contact could be made to the buried layer. The $N^+$ source regions were formed by nitrogen implantation (dose=$1.6\times10^{15}$ $cm^{-2}$). Different N-channel doses in the range of $1\times10^{12}$ to $2\times10^{13}$ $cm^{-2}$ were used to study the effect of N-channel dose on the device characteristics. All implants were annealed at 1400 °C in argon for 30 minutes. Al ohmic contacts were made to the $P^+$ regions using RTA at 900 °C for 60 sec. Ti/Al was used for ohmic contacts to the $N^+$ source and drain regions and simultaneously to form the Schottky gate contacts to the $N^-$ regions to reduce process complexity.

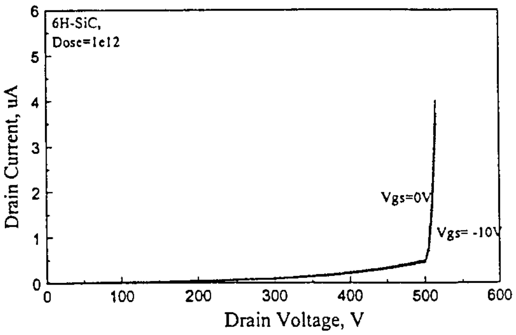

Fig.5 Output characteristics of a typical 6H-SiC MESFET with N-channel dose of 1e12/cm².

***Experimental Results:*** All the devices were characterized using a Keithley model 251 system at room temperature. The devices with less than 2x$10^{12}$ cm$^{-2}$ dose N-channel implant were normally-off as shown in Fig.5 and had very high on-resistance at zero gate bias due to the absence of a conducting channel. The on-state performance of these devices could not be improved even by applying a positive gate bias since the maximum positive gate bias was limited to about 2V, beyond which the gate current increased rapidly. However, the devices with high N-channel doses beyond 1x$10^{13}$ cm$^{-2}$ had good on-state conduction characteristics. Hence only the results obtained on the 1x$10^{13}$ and 2x$10^{13}$ cm$^{-2}$ dose devices are reported below. Since the devices on 6H-SiC and 4H-SiC had different characteristics, they are discussed separately.

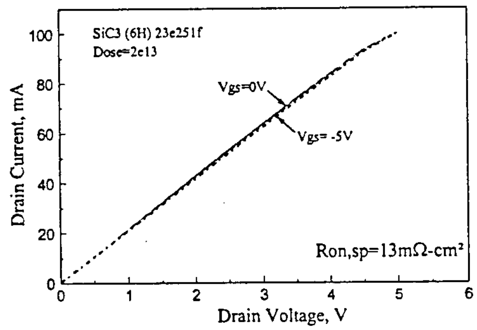

Fig.6 (b) Measured on-state I-V characteristics of the 6H-SiC MESFET (dose=2e13/cm²)

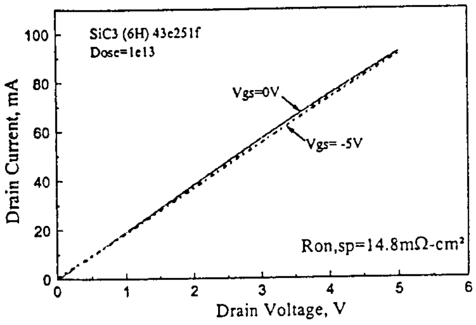

Fig.6 (a) Measured on-state I-V characteristics of the 6H-SiC MESFET (dose=1e13/cm²)

***6H-SiC MESFETs:*** Figures 6 (a) and (b) show the on-state I-V characteristics of typical 6H-SiC devices fabricated using channel implant doses of 1x$10^{13}$ and 2x$10^{13}$ cm$^{-2}$. It can be seen that the devices are normally-on with very good conduction at zero gate bias. They had excellent specific on-resistance of 14.8 mΩ-cm$^2$ for channel dose of 1x$10^{13}$ cm$^{-2}$ and 13 mΩ-cm$^2$ for channel dose of 2x$10^{13}$ cm$^{-2}$. It is worth pointing that the ideal $R_{on,sp}$ is

3.2 mΩ-cm$^2$ (for 10μm, 2.5x10$^{16}$ cm$^{-3}$ doped epilayer) and hence the specific on-resistance of the fabricated devices is only 4X higher than the ideal value. The measured specific on-resistance is higher than the ideal value due to the contributions from the channel, JFET and substrate resistances, of which the channel is the most significant and can be reduced by increasing the channel dose. It may be noted that the on-resistance decreased with increasing N-channel dose as expected. However, it was observed that the gate bias had only little effect on the drain current for these devices fabricated with high channel dose and these devices could not be taken to the blocking mode. It was found that the gate contact was very leaky under reverse bias, as shown in Fig.7, which made it impossible to pinch off the channel. We believe that the high dose channel implants increased the surface concentration at the Schottky interface resulting in high reverse leakage currents for the Schottky junction. Attempts to pinch off the channel by applying negative bias to the buried P$^+$ gate were unsuccessful due to the metal gate acting as a channel bypass for current conduction. Thus even though, we were able to get excellent on-state conduction with the higher doses as expected, the blocking characteristics were severely compromised. High channel doses are required to get good on-state conduction, however this results in increasing the surface concentration at the Schottky gate contact leading to a leaky gate. The gate leakage current can be reduced by using a high barrier (>1eV) Schottky contact metal to form the gate contact. This will result in increased process complexity as a multiple metal process may have to be used to achieve this.

***4H-SiC MESFETs:*** The on-state I-V characteristics of two typical 4H-SiC devices fabricated with two channel implant doses are shown in Fig.8 (a) and (b). It can be seen

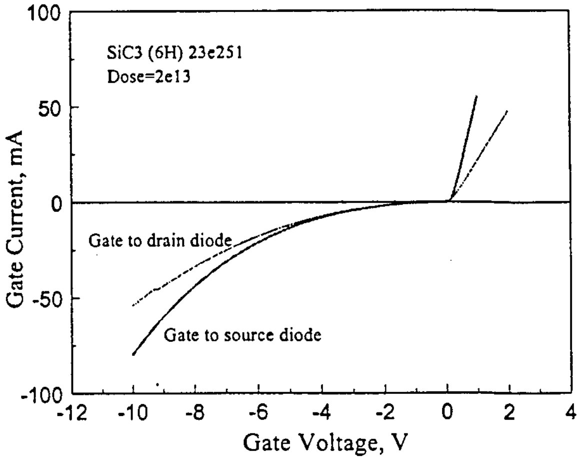

Fig.7 The I-V characteristics of typical Gate to Source and Gate to Drain diodes on 6H-SiC devices.

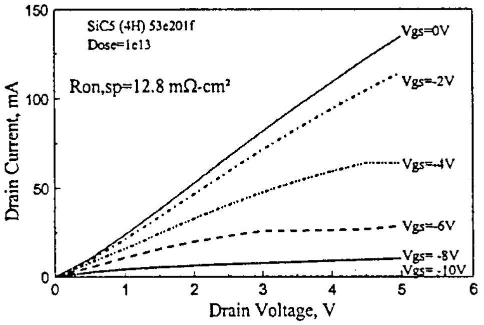

Fig.8 (a) Measured on-state I-V characteristics of the 4H-SiC MESFET (dose=1e13/cm²)

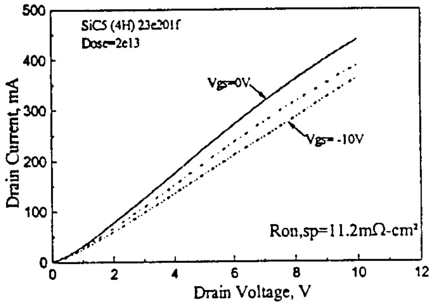

Fig.8 (b) Measured on-state I-V characteristics of the 4H-SiC MESFET (dose=2e13/cm²)

that both the devices are normally-on with good conduction at zero gate bias. They had low specific on-resistance of 12.8 mΩ-cm$^2$ for the channel dose of 1x10$^{13}$ cm$^{-2}$ and 11.2 mΩ-cm$^2$ for the channel dose of 2x10$^{13}$ cm$^{-2}$. Calculations show that the ideal $R_{on,sp}$ is 0.42 mΩ-cm$^2$ (for 10μm, 1.6x10$^{16}$ cm$^{-3}$ doped epilayer) and hence the specific on-resistance of the fabricated devices is much higher (~30X) than the ideal value. Good gate control was observed on the devices fabricated with channel dose of 1x10$^{13}$ cm$^{-2}$ as shown in Fig.8(a). However, these devices could block only 15V due to the breakdown of the Schottky diode between gate and drain at about 25V as shown in Fig.9. For the devices which had the higher (2x10$^{13}$ cm$^{-2}$) dose implant, the gate had little control over the drain current due to the higher channel concentration. These devices could not be taken to the blocking mode of operation as the Schottky gate breaks down at around 20V, even before the channel could be pinched off.

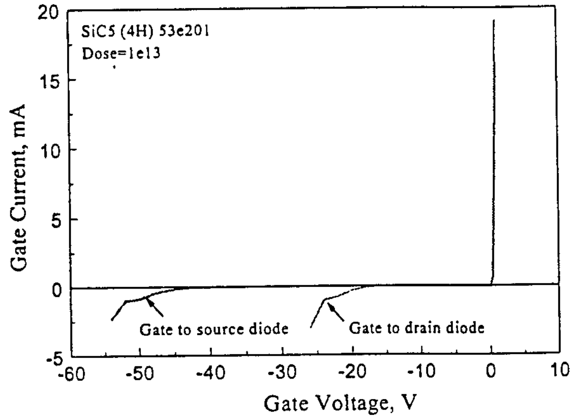

Fig.9 The I-V characteristics of typical Gate to Source and Gate to Drain diodes on 4H-SiC MESFETs.

***Conclusions:*** Planar lateral channel SiC MESFETs with low specific on-resistances were proposed and experimentally demonstrated. The on-resistance decreased with increasing N-channel dose for both 6H- and 4H-SiC devices. Even though increasing the channel dose improved the on-state characteristics, the blocking voltage reduced significantly. This shows that the channel has to be optimized very carefully to obtain good forward conduction and blocking characteristics. Gate controlled current saturation was observed on 4H-SiC MESFETs with $1x10^{13}$ $cm^{-2}$ dose channel implant, though the device had low blocking voltage. The high channel dose devices on both 6H- and 4H-SiC wafers had good on-state characteristics, but they could not be turned off due to the leaky Schottky gate junction. By comparing the characteristics of the devices with the different doses, it is evident that the low dose devices have poor on-state characteristics but good blocking characteristics whereas the higher dose devices had excellent on-state drops but poor blocking characteristics. This shows that the value of N-channel dose is critical and a dose between $10^{12}$ and $10^{13}$ $cm^{-2}$ is required to give the best compromise between on-state and blocking characteristics.

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# GROWTH VIA HOT WALL CHEMICAL VAPOR DEPOSITION AND CHARACTERIZATION OF 6H- and 4H- SiC THIN FILMS

by

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## Abstract:

A hot wall SiC chemical vapor deposition system has been constructed for the growth and doping of 4H- and 6H-SiC thin films at very high temperatures and high growth rates. The design incorporates a separate load lock from which the growth chamber and a reflection high-energy electron diffraction (RHEED) chamber are attached. Essentially all the system hardware has been assembled. The installation of the electrical wiring and gas lines in the building and in the room in which the system will be housed is underway. Construction drawings for water connections have been completed and these items are being installed at this time. Upfitting of the laboratory to meet all safety codes for the use of silane is in the final stages of construction.

## 1. Description of Equipment

The system design is comprised of a six way cross, serving as a loadlock, from which two separate chambers are attached. A high temperature growth chamber and RHEED analysis chamber are attached on each side perpendicular to the axis of the loadlock. The latter chamber will be used to monitor film crystallinity, crystal structure and the formation of new surfaces. The sample will be transferred to and from the various chambers on a SiC coated graphite susceptor platform on which the sample will be placed. The transfer mechanism consists of a platform which is moved from chamber to chamber by means of a manipulator rod which is fastened to the side of the susceptor.

The growth chamber consists of a rotating module, to which the susceptor is attached. Growth will occur on the sample in an upside-down position, with gases flowing upward, while the susceptor is being rotated. The susceptor is attached to the rotating rod assembly by a groove into which the susceptor slides when transfer of the sample takes place. Once the sample is transferred to the rotating rod, the rod is brought down to the quartz portion of the reaction chamber. Here, the sample is heated via RF coil, and gases are introduced from the bottom of the reactor. A design which incorporates a graphite cylinder for hot wall CVD growth is in progress. The growth temperature will be monitored by means of a standing pyrometer mounted outside the quartz chamber and aimed at the sample. Growth processes parameters, such as gas flow rate and pressure, will be monitored by electronic components. Gas flow will be controlled by mass flow controllers and pressure by capacitance manometers.

The SiC growth process will consist of introducing $SiH_4$ and $C_2H_4$ as the reactive components in a $H_2$ carrier. Nominal flow values will be on the order of 1 to 10 sccm for each. Hydrogen carrier flow rates will be on the order of three liters per minute. Other reactant sources which will be attached to the system include $NH_3$ and an $N_2/H_2$ mixture for n-type doping and triethlyaluminum for and p-type doping.

## 2. Accomplishments to Date

- Design and construction of a SiC thin film growth system containing a load lock, growth chamber, RHEED analysis chamber and support frames.
- Three six-way crosses have been assembled with the adjoining gate valves on the frame, and available flanges and window ports have been attached.
- A quartz chamber-to-cross assembly has been machined which will provide a sealed interface between two parts of the growth chamber.

- Quartz cylinders have been cut to design dimensions.
- Flange parts, pressure gauge attachments, pump connection parts, and a rotating rod assembly, have been machined.
- An RF generator has been refurbished and returned and will be used to provide RF heating to the susceptor.
- Assembly of a switch panel to control the nupro valves and to enable computer control is complete.
- A RHEED chamber manipulator has being fitted with a holder which will accommodate the susceptor upon transfer.
- Electrical wiring of the switch panel to control the nupro valves has been assembled.
- Assembly of various gas lines on a panel to be mounted on one side of the system has been completed.
- Installation of electrical and water utilities for the system as well as safety changes in the laboratory are being performed at this time.
- A gas monitoring system is being installed for safe system operation.

## IV. Discussion

The proposed design was developed with many sources of input. A number of constraints determined the design configuration and materials used in the system.

One of the main concerns was the high operating temperature of the growth chamber. Temperatures of approximately 1600-1700°C will be used to grow the SiC films. Quartz was determined to be the best material for the growth portion of the chamber. A double-walled quartz vessel, water cooled around the perimeter, has been designed and constructed for optimum cooling. Discussions are underway at this time regarding the design of the most appropriate graphite inner chamber to place inside the quartz cylinders for achieving a SiC high growth rate.

Another concern was the transfer mechanism of the susceptor and the placement of samples on the susceptor surface. It was decided that small silicon carbide screws would be the most flexible for our purposes to accommodate various sized samples. For the transfer mechanism, a simple tongue-in-groove assembly, moved between chambers by means of a transfer arm which would screw into the side of the susceptor was deemed simplest and most practical.

## V. Conclusions/Future Research Plans and Goals

A system design for the deposition of SiC thin films has been developed. Essentially all components have been designed or received. Other needed parts are currently being machined. A graphite inner chamber is being devised to accommodate hot wall CVD growth. The final assembly of the system will be conducted when electrical and water sources to the laboratory are in place.